**Parity Generator and Checker:**

What is a Parity Bit?

A parity bit is a binary digit added to a set of data bits to help detect errors in data transmission or storage. It ensures that the total number of 1s in the data is either even (even parity) or odd (odd parity), depending on the chosen scheme.

**Parity Generator:**

A parity generator is a combinational logic circuit that adds a parity bit to a given binary message to ensure error detection during data transmission.

It does not correct errors, but helps detect single-bit errors.

It is of two types:

* Even parity generator.
* Odd parity generator.

**Even Parity generator:**

An even parity generator adds a parity bit such that the total number of 1’s (data bits + parity bit) is even.

P\_even = A ⊕ B ⊕ C ⊕ D

**Odd parity generator:**

An odd parity generator adds a parity bit such that the total number of 1’s (data bits + parity bit) is odd.

P\_odd = ¬(A ⊕ B ⊕ C ⊕ D)

**Truthtable:**

A sheet of paper with writing on it

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**Implemented Parity generators using Verilog on Xilinx vivado:**

**1.Even parity generator(data flow modelling):**

**Design**:

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A diagram of a computer

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**Test Bench:**

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A screen shot of a computer

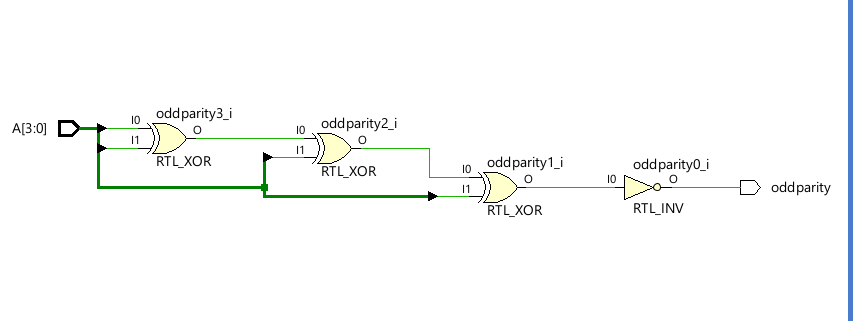
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**2.Odd parity generator(behavioural modelling):**

**Design:**

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**Test bench:**



A screenshot of a computer

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**Parity checker:**

A parity checker is a combinational logic circuit used at the receiver end to detect errors in transmitted data. It checks whether the received data (including the parity bit) conforms to the expected parity (even or odd).

It does not correct errors, only detects them.

It outputs a ‘0’ (no error) if parity is correct and ‘1’ (error) if parity is violated.

It is of two types:

* Even parity checker.
* Odd parity checker.

**1. Even Parity Checker**

Checks if the total number of 1’s in the received data (including parity bit) is even.

If total 1’s are even → no error

If total 1’s are odd → error detected

Check\_even = A ⊕ B ⊕ C ⊕ D ⊕ P

**2.Odd Parity Checker**

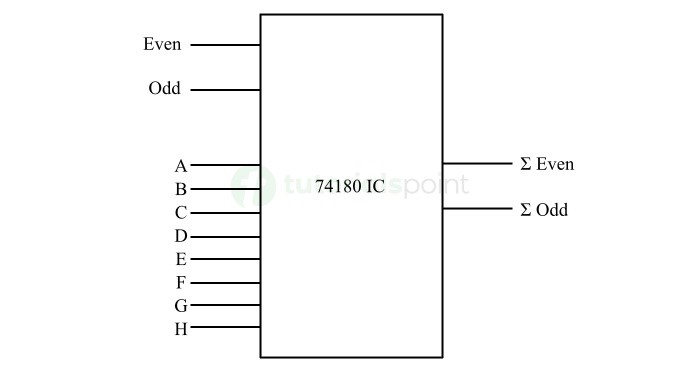
Checks if the total number of 1’s in the received data (including parity bit) is odd.

If total 1’s are odd → no error

If total 1’s are even → error detected

Check\_odd =~( A ⊕ B ⊕ C ⊕ D ⊕ P)

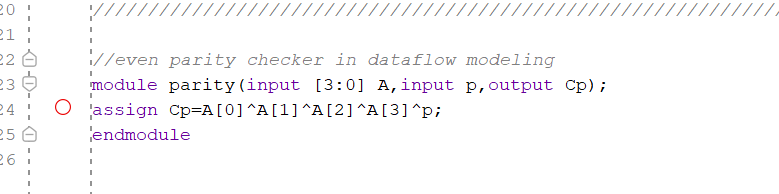
**IC 74180 9-Bit Parity Generators/Checkers**



**Implemented parity checkers using Verilog:**

**1.Even parity checker(data flow modelling):**

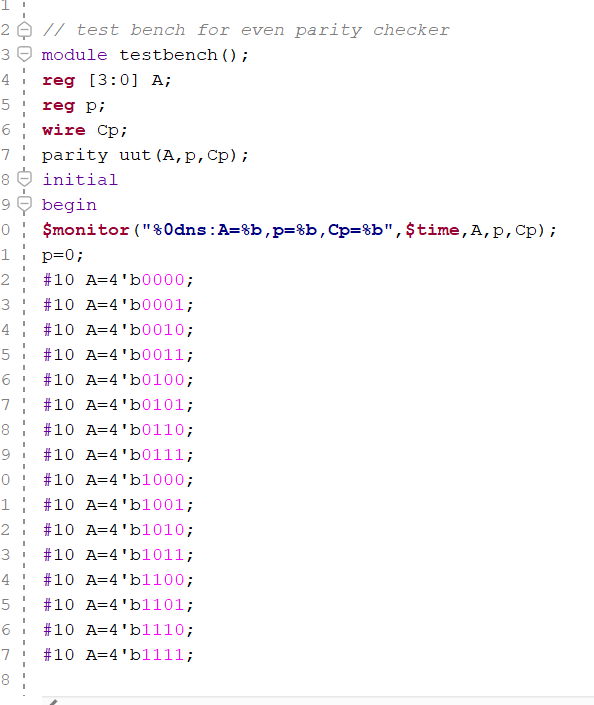
**Design:**



A diagram of a computer program

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**Test bench:**

A screenshot of a computer code

AI-generated content may be incorrect.

A screen shot of a computer

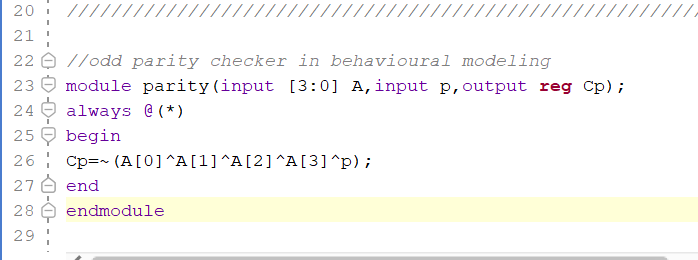
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A diagram of a computer circuit

AI-generated content may be incorrect.

**2.Odd parity chcker(behavioural modelling):**

**Design:**



A screen shot of a graph

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A screenshot of a computer program

AI-generated content may be incorrect.

**Test bench:**

